

**IN THE CLAIMS**

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

- 1           1.       (Original) A wireless transceiver device, comprising:  
2           modulation circuitry for modulating and demodulating signals that are transmitted over the  
3           airwaves;  
4           frequency conversion circuitry for up converting and down converting between radio frequency  
5           signals and baseband frequency signals;  
6           digital-to-analog conversion circuitry for converting from analog to digital and from digital to  
7           analog; a radio controller; and  
8           baseband processing circuitry including a first in, first out memory structure for storing addresses  
9           for accessing data blocks.
- 1           2. (Original) The wireless transceiver of claim 1 further including a plurality of command blocks  
2           formed within a memory structure, which command blocks include addresses of data blocks stored within  
3           random access memory.
- 1           3. (Original) The wireless transceiver of claim 2 wherein the first in, first out memory structure  
2           includes pointers that define addresses of the command blocks.
- 1           4. (Original) The wireless transceiver of claim 2 further forming a memory portion for storing an  
2           indicator for indicating whether a command block is in use.
- 1           5. (Previously presented) The wireless transceiver of claim 1 wherein the modulation circuitry  
2           includes Gaussian Phase Shift Keying modulation and demodulation circuitry.
- 1           6. (Previously presented) The wireless transceiver of claim 1 wherein the frequency conversion  
2           circuitry converts directly between radio frequency and baseband.

1           7. (Original) A method for storing and transmitting data, comprising:  
2           storing a data block in random access memory; and  
3           storing a pointer that corresponds to the data block in a first in, first out memory structure.

1           8. (Original) The method of claim 7 wherein the pointer comprises an address of a command  
2    block.

1           9. (Original) The method of claim 8 further including the step of storing an address of the data  
2    block in the command block.

1           10. (Original) The method of claim 9 further including the step of setting a signal in a defined  
2    memory location, which signal indicates that the address in the command block is for data that has yet to  
3    be successfully transmitted and therefore that the command block is busy.

1           11. (Original) The method of claim 10 wherein an address for a data block is only stored in a  
2    command block if an indicator reflects that the command block does not contain the address of a data  
3    block that has yet to be successfully transmitted.

1           12. (Original) The method of claim 7 further including the step of evaluating a command block  
2    address stored within a FIFO pointer.

1           13. (Original) The method of claim 12 further including examining the contents of the command  
2    block specified by the pointer to determine a data block address.

1           14. (Original) The method of claim 13 further including the step of evaluating at least the first  
2    memory location of the data block whose address is specified in the command block to determine the size  
3    of the data block.

1           15. (Original) The method of claim 14 further including the step of retrieving an amount of data  
2    corresponding to the size data block specified in claim 14 and transmitting that data to a radio modem for  
3    transmission over a wireless airwaves.

1           16. (Original) The method of claim 15 further including the step of resetting the indicator signal if  
2 the transmission was successful.

1           17. (Original) A memory structure formed within a baseband processing system, comprising: a  
2 random access memory portion for storing data blocks that are to be transmitted in a first in, first out  
3 order; and a first in, first out memory structure for storing pointers that correspond to the data blocks.

1           18. (Original) The memory structure of claim 17 wherein a plurality of command blocks are  
2 defined within the random access memory wherein each command block is for specifying an address of a  
3 data block that is to be transmitted.

1           19. (Original) The memory structure of claim 18 further including a defined memory portion for  
2 storing command block indicators for each command block, which indicators specify whether its  
3 corresponding command block includes the address of a data block that has yet to be transmitted  
4 successfully.

1           20. (Original) The memory structure of claim 19 wherein the memory portions for storing the  
2 indicators are each one bit in length.

1           21. (Original) The memory structure of claim 18 wherein the memory portions for storing the  
2 command blocks are each four bytes in length.

1           22. (Original) The memory structure of claim 17 wherein the first in, first out memory structure  
2 defines a plurality of first in, first out memory blocks wherein each first in, first out memory relates to  
3 data blocks that are to be transmitted to a particular device.